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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/930,202	08/16/2001	Takashi Ipposhi	212812US2	9227

22850 7590 04/26/2002

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EXAMINER

NGUYEN, JOSEPH H

ART UNIT PAPER NUMBER

2815

DATE MAILED: 04/26/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/930,202

Applicant(s)

IPPOSHI ET AL.

Examiner

Joseph Nguyen

Art Unit

2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 16 August 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

## DETAILED ACTION

### *Drawings*

Figures 17-21 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 4, 5- 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over figures 17-21 of the acknowledged prior art (APA) in view of Yasue.

Regarding claim 1, (APA) discloses a semiconductor wafer comprising first and second semiconductor wafers 1, 3 having crystal orientation display sections...wherein said crystal orientation display sections are indicative of an identical crystal orientation in said first and second wafers and said first and second semiconductor wafers are bonded with said crystal orientation display sections. (APA) does not disclose nicks indicative of orientation formed on fringes. However, Yasue discloses on figure 1 nicks 23,24 indicative of orientation formed on fringes. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify (APA) by having nicks indicative of orientation formed on fringes for the purpose

of precisely identifying the crystal orientation of the semiconductor wafer as taught by Yasue (col. 4, lines 34-35).

Regarding claim 4, (APA) discloses the first semiconductor wafer 1 is a wafer for a support substrate.

Regarding claim 5, (APA) discloses a semiconductor wafer comprising a first semiconductor wafer 1; and a second semiconductor wafer having a crystal orientation display section ... wherein said first and second semiconductor wafers are bonded to each other such that a part of a main surface of said first semiconductor wafer is exposed to said crystal orientation display section of said semiconductor wafer, and printing is given to said part of said main surface of said first semiconductor wafer. (APA) does not disclose nicks indicative of orientation formed on a fringe. However, Yasue discloses on figure 1 nicks 23,24 indicative of orientation formed on a fringe. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify (APA) by having nicks indicative of orientation formed on fringes for the purpose of precisely identifying the crystal orientation of the semiconductor wafer as taught by Yasue (col. 4, lines 34-35).

Regarding claim 6, (APA) and Yasue together disclose the structure of claim 6.

Regarding claim 7, (APA) discloses the first semiconductor wafer 1 is a wafer for a support substrate, said second semiconductor wafer 3 is a wafer for an SOI layer, and an insulating film 2 is formed on a main surface of at least one of said wafer for the support substrate and said wafer for the SOI layer.

Regarding claim 8, (APA) discloses a semiconductor wafer comprising first and second semiconductor wafers 1, 3 having bulk structures, wherein said first and second semiconductor wafers are bonded with crystal orientations. (APA) does not disclose the crystal orientations shifted from each other. However, Yasue discloses on figure 1 the crystal orientations shifted from each other. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify (APA) by having the crystal orientations shifted from each other for the purpose of precisely identifying the crystal orientation of the semiconductor wafer as taught by Yasue (col. 4, lines 34-35).

Claims 2 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over (APA) and Yasue as applied to claims 1 and 8 above, and further in view of (JP9-246505).

Regarding claims 2 and 9, (APA) discloses substantially all the structures set forth in the claimed invention except the crystal orientation display sections shifted from each other by 45 degrees. However, (JP9-246505) discloses the crystal orientation display sections shifted from each other by 45 degrees (see Abstract of JP9-246505). In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify (APA) and Yasue by having the crystal orientation display sections shifted from each other by 45 degrees for the purpose of improving the wafer bonding process of a semiconductor wafer.

Claims 3 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over (APA) and Yasue as applied to claims 1 and 8 above, and further in view H. Sayama et al.

Regarding claims 3 and 10, (APA) discloses substantially all the structures set forth in the claimed invention except a channel direction between a source and drain being parallel with a direction of a crystal orientation  $\langle 100 \rangle$ . However, H. Sayama et al discloses on figure 4b a channel direction between a source and drain being parallel with a direction of a crystal orientation  $\langle 100 \rangle$ . In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify (APA) and Yasue by having a channel direction between a source and drain being parallel with a direction of a crystal orientation  $\langle 100 \rangle$  for the purpose of improving the current drivability of pMOSFET as taught by H. Sayama et al (See Abstract of H. Sayama et al).

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent 3920492 to Sugita et al discloses a semiconductor device.

US Patent 6174222 B1 to Sato et al disclose the fabrication of a semiconductor IC device.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Nguyen whose telephone number is (703) 308-1269. The examiner can normally be reached on Monday-Friday, 7:30 am- 4:30 pm

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 308-7382 for regular communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JN  
April 11, 2002

A handwritten signature in black ink, appearing to read 'Eddie Lee', is positioned above the printed name and title.

**EDDIE LEE**  
**SUPERVISORY PATENT EXAMINER**  
**TECHNOLOGY CENTER 2800**